corrosion easily occurs. When a dummy fine line pattern is formed, so that an area ratio of the dummy fine line pattern to the entire wire patterns including a fine line pattern, a large pad pattern and the dummy fine line pattern, is larger than an area ratio of the fine line pattern to the entire wire patterns including the fine line pattern, the large pad pattern, and the dummy fine line pattern, the corrosion of the fine line pattern can be prevented.--

IN THE CLAIMS

Please amend claims 1, 3-5 and 7-11 to read as follows:

1. (Amended) A semiconductor device comprising:

a plurality of metal wire patterns which include a fine line pattern and pad patterns, an area of the fine line pattern being more than 1% of a total area of said plurality of metal wire patterns.

3. (Amended) The semiconductor device as recited in claim 1, wherein the pad patterns include connection pad patterns which electrically connect the pad patterns to the fine line pattern, said connection pad patterns being included in said total area.

4. (Amended) The semiconductor device as recited in claim 1, wherein the plurality of metal wire patterns are made of aluminum or copper.

5. (Amended) A semiconductor device comprising:

a plurality of metal wire patterns which include main fine line patterns, main pad patterns and dummy fine line patterns, an area of the dummy fine line patterns, which are connected to the pad patterns, being less than 1% of a total area of said plurality of metal wire patterns and also being less than a value obtained by dividing an area of the main fine line patterns by said total area.

7. (Amended) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns are made of aluminum or copper wire.

8. (Amended) The semiconductor device as recited in claim 5, wherein the dummy fine line patterns do not form or contribute to any electric circuit.

9. (Amended) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns further include dummy pad patterns, to which the dummy fine line patterns are connected, said dummy pad patterns and said dummy fine line patterns being electrically disconnected from the main fine line patterns and the main pad patterns.

10. (Amended) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns further include dummy pad pool patterns, to which the dummy fine line

patterns are connected, said dummy pad pool patterns and said dummy fine line patterns being electrically disconnected from the main fine line patterns and the main pad patterns.

11. (Amended) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns are made of aluminum or copper wire.

Please add the following claims:

--12. The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns further include connection pad patterns which electrically connect the main pad patterns to the fine line patterns, said connection pad patterns being included in said total area.

13. The semiconductor device as recited in claim 12, wherein the total area is represented by Ap+Ac+A+d, where, 'd' represents the area of the dummy fine line patterns, 'Ap' represents an area of the main pad patterns, 'Ac' represents an area of the connection pad patterns and 'A' represents the area of the main fine line patterns.--